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EXAMINER	
LEWIS, DAVID LEE	
ART UNIT	**PAPER NUMBER**
2673	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,436	YOSHIHARA ET AL.	
	Examiner	Art Unit	
	David L. Lewis	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. (6489952).

As in claims 1, Tanaka et al. teaches of a liquid crystal device comprising: a liquid crystal material characterized by spontaneous polarization, **column 25 lines 1-13**,

being responsive to an applied signal for writing data and controlling a light transmittance of said material, wherein a voltage of said signal, corresponding to an image to be displayed and switched by thin film transistor, is offset to either a single, positive or negative constant level from 0 V at said material at all times during operation, except during signal application, **column 6 lines 25-40, column 7 lines 43-51, column 8 lines 45-58**.

Wherein as shown in figures 1 and 4, the com1 signal line is driven alternately to the com2 signal line, both lines being driven with an offset value for the purpose of making the voltage applied to the image pixel low. The signal line com1 alternates polarity corresponding to when the odd line is driven for display and the offset is determined by the constant com1 or com2 signal during each frame.

As in claims 2, Tanaka et al. teaches of wherein said signal is offset positively or negatively so that a light transmission through said liquid crystal material being driven by said signal becomes to be blocked, **column 8 lines 45-58**, wherein the potential is of the counter electrode is made opposite the image signal, said light transmission being alternately blocked in relation to driving odd and even groups.

As in claims 3, Tanaka et al. teaches of liquid crystal device comprising: a first substrate including a first electrode on a first face thereof, **figure 18B items 1771 and 1772**;

a second substrate including a second electrode on a second face thereof, wherein said second substrate and said first substrate are sealed spaced apart so that said first and second face each other, **figure 17A item 1701**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 18B item 1774, column 25 lines 1-13**;

a first voltage generating circuit for supplying a voltage to said first electrode, **figure 1 item COM, column 8 lines 30-37**;

and a data signal circuit for supplying a data pulse to said second electrode, **figure 4 item S1-Sn**,

wherein a voltage across said liquid crystal between said first and second electrodes is offset to either a single, positive or negative constant level from a reference voltage of said device at all times during operation, except during said data pulse being applied, **column 8 lines 45-58**.

Wherein as shown in figures 1 and 4, the com1 signal line is driven alternately to the com2 signal line, both lines being driven with an offset value for the purpose of making the voltage applied to the image pixel low. The signal line com1 alternates polarity corresponding to when the odd line is driven for display.

As in claims 4, Tanaka et al. teaches of wherein said data pulse is offset positively or negatively so that a light transmission through said liquid crystal material being driven by said pulse becomes to be blocked, column 8 lines 45-58, wherein the potential is of the counter electrode is made opposite the image signal, said light transmission being alternately blocked in relation to driving odd and even groups..

As in claims 5, Tanaka et al. teaches of wherein said second substrate having an active element electrically connected to said second electrode so as to electrically control a picture element, figure 18A item 1701 (active matrix circuit).

As in claims 6, Tanaka et al. teaches of wherein said voltage supplied by said first voltage generating circuit is offset so that a voltage across said liquid crystal material between said first and second electrodes is kept positively or negatively to said reference voltage of said device except during said data pulse being applied, **column 8 lines 45-58**. Wherein as shown in figures 1 and 4, the com1 signal line is driven alternately to the com2 signal line, both lines being driven with an offset value for the purpose of making the voltage applied to the image pixel low. The signal line com1 alternates polarity corresponding to when the odd line is driven for display..

As in claims 7, Tanaka et al. teaches of liquid crystal panel comprising: a first substrate including a first electrode on a first face thereof, **figure 18B items 1771 and 1772**;

a second substrate including a second electrode on a second face thereof, wherein said second substrate and said first substrate are sealed spaced apart so that said first and second face each other, **figure 17A item 1701**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 18B item 1774, column 25 lines 1-13**;

a first voltage generating circuit for supplying a voltage to said first electrode, **figure 1 item COM, column 8 lines 30-37**;

a data signal circuit for supplying a data pulse to said second electrode, **figure 1 item 101**, **figure 4 item S1-Sn**;

and a light source for emitting more than monochromatic lights, each of said monochromatic lights being emitted time divisionally toward said first or second substrates, **column 2 lines 15-25, column 28 lines 35-45**,

wherein a voltage across said liquid crystal material between said first and second electrodes is offset to either a single, positive or negative constant level from a reference voltage of said device at all times during operation, during except said during said data pulse application when an image is displayed, **column 8 lines 45-58**.

As in claims 8, Tanaka et al. teaches of liquid crystal panel comprising: a first substrate including a first electrode on a first face thereof, **figure 18B items 1771 and 1772**;

a second substrate including a second electrode on a second face thereof, wherein said second substrate and said first substrate are sealed spaced apart so that said first and second face each other, **figure 17A item 1701**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 18B item 1774, column 25 lines 1-13**;

a first voltage generating circuit for supplying a voltage to said first electrode, **figure 1 item COM, column 8 lines 30-37**;

a data signal circuit for supplying a data pulse to said second electrode, **figure 1 item 101**, **figure 4 item S1-Sn**;

and polarizer films provided on each outer face of said first and second substrates, **column 24 lines 15-35**, **column 28 lines 35-45**,

wherein a voltage across said liquid crystal material between said first and second electrodes is offset to either a single, positive or negative constant level from a reference voltage of said panel at all times during operation except during said data pulse application so that said liquid crystal material blocks a light transmission through said liquid crystal material when the image is displayed, **column 8 lines 45-58**,

wherein the potential is of the counter electrode is made opposite the image signal, said light transmission being alternately blocked in relation to driving odd and even groups.

As in claims 9, Tanaka et al. teaches of liquid crystal display panel comprising: a first substrate including a common electrode on a first face thereof, **figure 18B items 1771 and 1772,**

a second substrate including data signal electrodes, **figure 1 item 101**, scanning electrodes, **figure 1 item 102**,

and switching elements which are connected to one of said data signal electrodes and one of said scanning electrodes on a second face thereof, **figure 1 item (1,1)**,

wherein said second substrate and said first substrate are sealed spaced apart so that said first and second faces face each other, **figure 18B items 1771 and 1701**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 18B item 1774**;

a common reference voltage generating circuit for defining a reference voltage of said data signal electrode, **column 8 lines 30-55**;

and a common electrode voltage generating circuit for supplying a voltage to said common electrode, wherein said common voltage is offset to either a single, positive or negative constant voltage at all times during operation when an image is displayed, **column 6 lines 25-40, column 8 lines 30-55,**

wherein said common voltage generating circuit is not shown, however is inherent to the shown system given the signals produced, figure 4, by on the shown display, **figure 1**.

As in claims 10, Tanaka et al. teaches of wherein said liquid crystal material having spontaneous polarization is ferroelectric liquid crystal material, column 25 lines 1-13.

As in claims 11, Tanaka et al. teaches of wherein said first substrate has a color filter, **column 28 lines 35-45**.

As in claims 12, Tanaka et al. teaches of liquid crystal display panel comprising: a first substrate including a common electrode on a first face thereof, **figure 18B items 1771 and 1772**;

a second substrate including data bus lines, **figure 1 item 101**,

scanning bus lines, **figure 1 item 102**,

and switching elements which are connected to one of said data bus lines and one of said scanning bus lines on a second face thereof, **figure 1 item (1,1),**

wherein said second substrate and said first substrate are sealed spaced apart so that said first and second faces face each other, **figure 18B items 1771 and 1701**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 18B item 1774**;

and a common electrode voltage generating circuit for supplying a voltage to said common electrode, **column 6 lines 25-40, column 8 lines 30-55,**

wherein said common voltage generating circuit is not shown, however is inherent to the shown system given the signals produced, figure 4, by on the shown display, **figure 1 item COM1**;

and a common reference voltage generating circuit for defining a reference voltage of said data bus lines, wherein said reference voltage is offset to either a single positive or negative voltage at all times during operation when the image is displayed, **column 6 lines 25-40, column 8 lines 30-55,**

wherein said common voltage generating circuit is not shown, however is inherent to the shown system given the signals produced, figure 4, by on the shown display, **figure 1, item COM2**.

As in claims 13, Tanaka et al. teaches of wherein said liquid crystal material having spontaneous polarization is ferroelectric liquid crystal material, column 25 lines 1-13.

As in claims 14, Tanaka et al. teaches of wherein said first substrate has a color filter, column 28 lines 35-45.

As in claims 15, Tanaka et al. teaches of further comprising: polarizer films provided on each outer faces of said first and second substrate, wherein said common voltage is offset so as that a light transmission of said liquid crystal material becomes to be block, column 24 lines 15-35.

As in claims 16, Tanaka et al. teaches of further comprising: a light source emitting a plurality of monochromatic colors, wherein each monochromatic color is emitted by said light source time divisionally in synchronism with an operation of said liquid crystal display panel, column 2 lines 15-23, column 28 lines 35-45.

As in claim 17, Tanaka et al. teaches of a liquid crystal device comprising: a first substrate including a first electrode on a first face thereof, **figure 18B items 1771 and 1772**;

a second substrate including a second electrode on a second face thereof, wherein said second substrate and said first substrate are sealed spaced apart so that said first and second substrates face each other, **figure 18B items 1771 and 1701**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 18B item 1774**;

a first voltage generating circuit for supplying a voltage to said first electrode, **figure 1 item com1, column 6 lines 25-35 (while not shown said circuit is inherent to said signal source)**;

and a data signal circuit for supplying a data pulse to said second electrode, **figure 1 item 101**,

wherein a voltage across said liquid crystal between said first and second electrodes is offset to either a single, positive or negative constant level form a reference voltage., **column 8 lines 47-58**.

Where the offset value is determined by the constant COM1 or COM2 signal during each frame.

2. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Hasegawa et al. (2001/0011979 A1).

As in claims 1, Hasegawa et al. teaches of a liquid crystal device comprising: a liquid crystal material characterized by spontaneous polarization, **paragraph 84**,

being responsive to an applied signal for writing data and controlling a light transmittance of said material, **figure 11 item Vcom**,

wherein a voltage of said signal, corresponding to an image to be displayed and switched by thin film transistor, is offset to either a positive or negative constant level from 0 V at said material at all times during operation, except during signal application, **paragraph 117 and 143**.

As in claims 3, Hasegawa et al. teaches of liquid crystal device comprising: a first substrate including a first electrode on a first face thereof, **figure 10 items 15 and 17**;

a second substrate including a second electrode on a second face thereof, **figure 10 item 11 and 13**,

wherein said second substrate and said first substrate are sealed spaced apart so that said first and second face each other, **figure 10 item 11 and 15**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 10 item 21**;

a first voltage generating circuit for supplying a voltage to said first electrode, **figure 2 item 35**;

and a data signal circuit for supplying a data pulse to said second electrode, **figure 2 item 33**,

wherein a voltage across said liquid crystal between said first and second electrodes is offset to either a positive or negative constant level from a reference voltage of said device at all times during operation, except during said data pulse being applied, **paragraph 117 and 143**.

As in claims 7, Hasegawa et al. teaches of liquid crystal panel comprising: a first substrate including a first electrode on a first face thereof, **figure 10 items 15 and 17**;

a second substrate including a second electrode on a second face thereof, **figure 10 item 11 and 13,**

wherein said second substrate and said first substrate are sealed spaced apart so that said first and second face each other, **figure 10 item 11 and 15**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 10 item 21, paragraph 84**;

a first voltage generating circuit for supplying a voltage to said first electrode, **figure 2 item 35**;

a data signal circuit for supplying a data pulse to said second electrode, **figure 2 item 33**;

and a light source for emitting more than monochromatic lights, each of said monochromatic lights being emitted time divisionally toward said first or second substrates, **paragraph 84 and 174**,

(said time divisionally implied but not shown) wherein a voltage across said liquid crystal material between said first and second electrodes is offset to either a positive or negative constant level from a reference voltage of said device at all times during operation, during except said during said data pulse application when an image is displayed, **paragraph 117 and 143**.

As in claims 8, Hasegawa et al. teaches of liquid crystal panel comprising: a first substrate including a first electrode on a first face thereof, **figure 10 items 15 and 17**;

a second substrate including a second electrode on a second face thereof, **figure 10 item 11 and 13,**

wherein said second substrate and said first substrate are sealed spaced apart so that said first and second face each other, **figure 10 item 11 and 15**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 10 item 21, paragraph 84**;

a first voltage generating circuit for supplying a voltage to said first electrode, **figure 2 item 35**;

a data signal circuit for supplying a data pulse to said second electrode, **figure 2 item 33**;

and polarizer films provided on each outer face of said first and second substrates, **figure 10 item 22a,b**,

wherein a voltage across said liquid crystal material between said first and second electrodes is offset to either a positive or negative constant level from a reference voltage of said panel at all times during operation, except during said data pulse application so that said liquid crystal material blocks a light transmission through said liquid crystal material when the image is displayed, **paragraph 117 and 143**.

As in claims 9, Hasegawa et al. teaches of liquid crystal display panel comprising: a first substrate including a common electrode on a first face thereof, **figure 10 items 15 and 17,**

a second substrate including data signal electrodes, **figure 10 item 11 and 13**,

scanning electrodes, **figure 10 item 43**,

and switching elements which are connected to one of said data signal electrodes and one of said scanning electrodes on a second face thereof, **figure 3 item 12**,

wherein said second substrate and said first substrate are sealed spaced apart so that said first and second faces face each other, **figure 10 item 11 and 15, paragraph 84**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 10 item 21, paragraph 84**;

a common reference voltage generating circuit for defining a reference voltage of said data signal electrode, **figure 2 item 30 and 35**;

and a common electrode voltage generating circuit for supplying a voltage to said common electrode, wherein said common voltage is offset to either a positive or negative constant voltage at all times during operation when an image is displayed, **figure 2 item 30 and 35, paragraph 117 and 143.**

As in claims 12, Hasegawa et al. teaches of liquid crystal display panel comprising: a first substrate including a common electrode on a first face thereof, **figure 10 items 15 and 17**;

a second substrate including data bus lines, **figure 10 item 11 and 13**,

scanning bus lines, **figure 10 item 43**,

and switching elements which are connected to one of said data bus lines and one of said scanning bus lines on a second face thereof, **figure 3 item 12,**

wherein said second substrate and said first substrate are sealed spaced apart so that said first and second faces face each other, **figure 10 item 11 and 15, paragraph 84**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 10 item 21, paragraph 84**;

and a common electrode voltage generating circuit for supplying a voltage to said common electrode, **figure 2 item 30 and 35**;

and a common reference voltage generating circuit for defining a reference voltage of said data bus lines, wherein said reference voltage is offset to either a positive or

negative voltage at all times during operation when the image is displayed, **figure 2 item 30 and 35, paragraph 117 and 143.**

As in claim 17, Hasegawa et al. teaches of a liquid crystal device comprising: a first substrate including a first electrode on a first face thereof, **figure 10 items 15 and 17**;

a second substrate including a second electrode on a second face thereof, **figure 10 item 11 and 13,**

wherein said second substrate and said first substrate are sealed spaced apart so that said first and second substrates face each other, **figure 10 item 11 and 15, paragraph 84**;

a liquid crystal material having spontaneous polarization filled in a space between said first and second substrates, **figure 10 item 21, paragraph 84**;

a first voltage generating circuit for supplying a voltage to said first electrode, **figure 2 item 35**;

and a data signal circuit for supplying a data pulse to said second electrode, **figure 2 item 33**,

wherein a voltage across said liquid crystal between said first and second electrodes is offset to either a positive or negative constant level form a reference voltage at all times during operation, **paragraph 117 and 143.**

As in claims 2 and 4, Hasegawa et al. teaches of wherein said signal is offset positively or negatively so that a light transmission through said liquid crystal material being driven by said signal becomes to be blocked, paragraph 117 and 143.

As in claims 5, Hasegawa et al. teaches of wherein said second substrate having an active element electrically connected to said second electrode so as to electrically control a picture element, figure 3 item 12.

As in claims 6, Hasegawa et al. teaches of wherein said voltage supplied by said first voltage generating circuit is offset so that a voltage across said liquid crystal material between said first and second electrodes is kept positively or negatively to said reference voltage of said device except during said data pulse being applied, paragraph 117 and 143.

As in claims 10, Hasegawa et al. teaches of wherein said liquid crystal material having spontaneous polarization is ferroelectric liquid crystal material, paragraph 84.

As in claims 11 and 14, Hasegawa et al. teaches of wherein said first substrate has a color filter, paragraph 84.

As in claims 13, Hasegawa et al. teaches of wherein said liquid crystal material having spontaneous polarization is ferroelectric liquid crystal material, paragraph 84.

As in claims 15, Hasegawa et al. teaches of further comprising: polarizer films provided on each outer faces of said first and second substrate, wherein said common voltage is offset so as that a light transmission of said liquid crystal material becomes to be block, figure 10 items 22a,b, paragraph 85, paragraph 117 and 143.

As in claims 16, Hasegawa et al. teaches of further comprising: a light source emitting a plurality of monochromatic colors, wherein each monochromatic color is emitted by said light source time divisionally in synchronism with an operation of said liquid crystal display panel, paragraph 84 and 174.

Response to Arguments

3. Applicant's arguments filed on 8/2/2005 with respect to claims 1-17 have been considered and are not persuasive. Applicant has amended the claims to include language wherein the offset is either a single, positive or negative constant level from 0V at said material at all times during operation. This is the case for the Tanaka et al. reference **at all times during the operation of a frame period**. During each frame period the offset is either a single, positive or negative constant level from 0V as claimed. Where the offset value is determined by the constant COM1 or COM2 signal during each frame. As known in the art of displays the operation of a display can be performed in a single frame or multiple frames. Further, the common line may alternate or stay constant as well known in the art. Said alternation may assist with flicker or providing a low drive voltage. Hasegawa continues to read on the claims as previously argued. Rejection Maintained.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tanaka et al. (6163360).

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and

any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis

December 8, 2005

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600